A Simple Negative Impedance Circuit with No Internal Bias Supplies and Good Linearity

This communication presents a very simple and stable negative impedance circuit with no internal-bias supplies. The linearity is good over a wide operating range in spite of its simplicity. The characteristics of the circuit are essentially independent of transistor parameters if the transistors have typically large betas. The v-i characteristic of the circuit is essentially constant from dc to the order of the β-cutoff frequency of the transistors.

The configuration of the circuit is shown in Fig. 1. The two-transistor, three-resistor circuit has the negative impedance characteristics shown in the oscillogram of Fig. 2. The essentially piecewise-linear characteristic has three regions, the positive impedance region I, the negative impedance region II and the saturation region III. In region II the value of the negative impedance is primarily determined by the values of the passive component in the circuit as explained later. The resistor R_c improves the linearity but is not essential. The circuit can be regarded as a two-stage complementary dc amplifier with positive current feedback. Hence the circuit responds to zero frequency. The feedback ratio is determined by $R/r = n$ since the base voltage of the first transistor Q_1 is essentially constant when the two transistors operate in the active region, and the two-stage amplifier composed of Q_1 and Q_2 has large current gain. As a result the circuit shows a negative impedance of $-R_1/n$. This situation is better explained by Fig. 3 with the assumption that the transistors are idea; i.e., the common-base current gain is unity and the voltage between base and emitter is zero. Let us assume in Fig. 3 that the current i is flowing as a result of the voltage V applied between terminals 1 and 2. Since the common base current gain of transistor Q_1 is unity its base current should be zero. Hence the current i should flow through the resistor R and develop the voltage $-Ri = -nri$ across the point P and the ground. This voltage is equal to the voltage across the resistor r since the base-emitter voltage of Q_1 is zero. Thus we have

$$(i_{c2} + i)r = -nri. \quad (1)$$

Also

$$V = R_1 \cdot i. \quad (2)$$

Since the common base current gain of the second transistor Q_2 is also unity, the total current flowing into the circuit is

$$I = i + i_{c2}$$
$$= i + i(-n - 1) = -ni. \quad (3)$$

Hence, the impedance of the circuit is

$$R_N \equiv V/I = -R_1/n \quad \text{or} \quad -R_1 \frac{r}{R}. \quad (4)$$

Note that similar relations hold when R_1, R, and r are impedances instead of resistors. Note also that if resistor R_1 is replaced by an impedance z, (4) indicates that the circuit may be regarded as a negative impedance converter with the termination impedance z having the conversion factor n. n is determined by the ratio of R and r, and is not necessary real. Indeed, one can design n to have the proper frequency characteristics to improve the frequency characteristics of the circuit. If the current gains are not unity but very close to unity, (4) becomes,

$$R_N \cong -\frac{R_1}{n} \Big/ \left[1 + \frac{n+1}{n} \cdot \frac{1-\alpha_2}{\alpha_2}\right]. \quad (5)$$

Manuscript received December 17, 1964; revised April 10, 1965. This work was done while author was a Visiting Research Associate under the support of Hitachi Central Research Laboratory, Japan. Space and facilities were provided by Nonr 225(44).

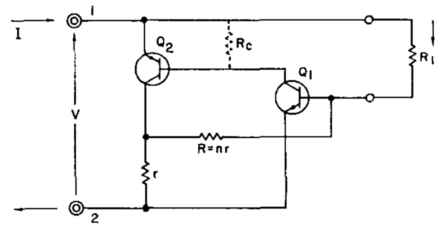
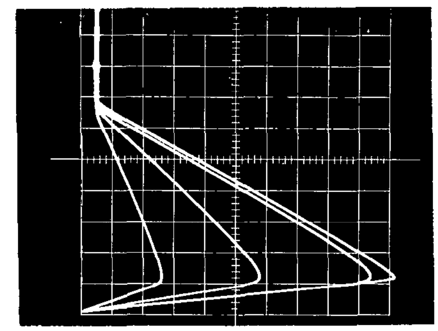


Fig. 1. The configuration of the simple negative impedance circuit.



HOR = 2V/DIV $\quad$ Q_1 = 2N706

VER = 1 MA/DIV $\quad$ Q_2 = 2N1991

r = 100 Ω

n = 5

Fig. 2. The v-i characteristics of the circuit. The circuit is essentially piecewise-linear, having three regions: I—the positive impedance region, II—the nagetive impedance region and III—the saturation region. The characteristics are controlled by the termination resistor R_1: from left to right R_1 = 6 $k\Omega$, 12 $k\Omega$ and 20 $k\Omega$. The linearity is improved by adding R_c: most right. R_c = 10 $k\Omega$ (R_1 = 20 $k\Omega$).

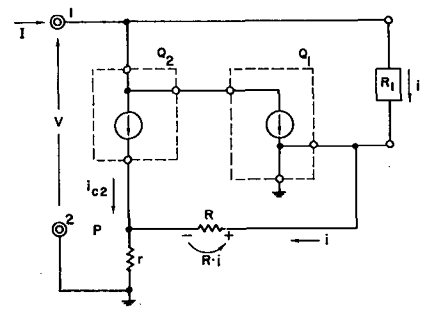


Fig. 3. The simplified equivalent circuit in region II.

Equation (5) indicates that the magnitude, linearity and frequency characteristics of α_2 is the most important factor. A more detailed analysis not given here shows that in order to have a good linear negative region and for (4) to be valid, the following conditions are necessary:[1]

(1) $\beta_1\beta_2 \gg n + 1$
(2) $R_1/r \gg n + 1$
(3) $n < 24$ (for silicon transistors at room temperature)

where β_1 and β_2 are the common emitter current gain of the transistors. The only requirement on transistor β is condition (1) which is easily met. No circuit adjustments are required when the above conditions are satisfied.

In region I, both transistors are in the cutoff condition, since the voltage between the base and emitter of Q_1 is either negative or too

[1] M. Nagata, "A simple negative impedance circuit with no internal bias supplies and good linearity," Stanford Electronics Labs. Rept. SEL-65-037 (TR 4813-5), Stanford University, Stanford, Calif., 1965.

small to induce the collector current. Hence all the current flows through R_1, R, and r. Thus the impedance of the curcuit is positive and has the value of

$$R_p \simeq R_1 + (n + 1)r. \tag{6}$$

As the voltage V is increased, the voltage between the base and emitter of Q_1, which is equal to $V(n + 1)r/R_p$, is also increased up to the value of E_b where the transistor Q_1 begins to conduct current. The value of E_b is approximately 0.6 volts for silicon transistors at room temperature. This critical value of V is given by

$$V_p(n + 1)r/R_p = E_b \tag{7}$$

which is the peak voltage of the circuit. If condition (2) exists, this peak voltage is given by

$$V_p \simeq E_b[R_1/(n + 1)r]. \tag{8}$$

The variation of the value of E_b in transistors of the same type is usually less than 30 mV. This means that V_p is constant within 5 per cent regardless of transistor change. Calculation shows that increasing β_2 decreases the effective E_b slightly:[1]

$$(\Delta E_b)_{\text{eff}} \simeq -\frac{kT}{q}\cdot\frac{\Delta\beta_2}{\beta_2} = -25\,\frac{\Delta\beta_2}{\beta_2}\,(\text{mV}). \tag{9}$$

A 20 per cent change in β_2 changes V_p less than 1 per cent; doubling β_2 changes it about -3 per cent. The experimental results showed that the maximum change of V_p was 9 per cent with transistors having $\Delta E_b \leqq 20$ mV and β_2 from 17 to 43. Even in this case no significant change of R_N is observed. R_N is essentially constant when condition (1) is valid, as indicated before. The maximum value of V_p is usually limited by the BV_{CEO} of Q_2. It was easy to design V_p from 2 to 50 V using a 2N709 for Q_1 and a 2N1991 for Q_2.

In region III, the transistors are both in the saturation region and the residual voltage V_s is determined by the saturation characteristics of the transistor pair:

$$V_s = (V_{EB2})_{\text{sat}} + (V_{CE1})_{\text{sat}}. \tag{10}$$

$(V_{EB})_{\text{sat}}$ is about 0.7 $\sim$ 0.8 volts for silicon transistors, whereas $(V_{CE1})_{\text{sat}}$ is less than 0.2 volts. Hence V_s is 1 volt or less. Note that increasing r does not increase V_s.

It should be noted that although the circuit of Fig. 1 resembles the practical form of current-inversion NIC given by A. I. Larky,[2] there is an important difference from it. The circuit given here satisfies the dc bias conditions by itself, hence operates down to dc with no additional component or internal bias supplies. Larky's practical form requires addition components or bias supplies for proper operation.

Summarizing, wide-range linear and stable negative impedance characteristics are achieved. Moreover, these characteristics are controlled by the choice of a resistor and are insensitive to transistor parameters. For example, in Fig. 2 a family of curves corresponding to different values of R_1 are shown, demonstrating that the circuit is operating as a negative impedance converter according to (4), (6), and (8). The circuit is simple and no internal bias supplies or circuit adjustments are required. The negative impedance region was useful from dc to several hundred kilocycles, and the linearity was better than ± 1 per cent using 50 per cent of the negative resistance region. The linearity is improved by adding R_c as shown in Fig. 2. The circuit has been successfully used as a negative resistance amplifier at 3 kc/s with a second harmonic content less than -40 dB, as a Wien-bridge type sine-wave oscillator at 1.6 kc/s with distortion less than -30 dB, as a relaxation oscillator and as a logic switching circuit element.[1]

ACKNOWLEDGMENT

The author wishes to thank Prof. J. G. Linvill of Stanford University for his stimulating discussions about the interpretation of the circuit as well as its applications.

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[2] A. I. Larky, "Negative impedance converters," *IEEE Trans. on Circuit Theory*, vol. CT-4, pp. 124–131, September 1957.

Comments on "Flow-Graph Evaluation of the Characteristic Polynomial of a Matrix"

In his communication, Milić[1] proposes a novel and ingenious procedure for evaluating the coefficients of the characteristic polynomial of a square matrix A. A particular advantage of this method lies in the fact that it does not require the expansion of a large number of determinants.

It is our purpose here to point out a method due to Danilevsky[2] that is simpler and easier to program for machine computation.

If a sequence of similarity transformations BAB^{-1} is performed upon the matrix A, the resultant matrix after each transformation will have the same eigenvalues and hence the same characteristic polynomial as A. The trick is to choose the matrix B in each transformation such that one ultimately obtains a matrix of the Frobenius canonical form, viz.

$$\begin{bmatrix} p_1 & p_2 & \cdots & p_{n-1} & p_n \\ 1 & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 \\ \hdashline 0 & 0 & \cdots & 0 & 0 \\ 0 & 0 & \cdots & 1 & 0 \end{bmatrix}.$$

Then $p(\lambda) = (-1)^n[\lambda^n - p_1\lambda^{n\ 1} - p_2\lambda^{n\ 2} \cdots - p_n]$.

The matrix B that produces the desired transformation is given by

$$\begin{bmatrix} & 0 & \cdots & 0 & 0 \\ 0 & 1 & \cdots & 0 & 0 \\ \hdashline \dfrac{-a_{n1}}{a_{n,n-1}} & \dfrac{-a_{n2}}{a_{n,n-1}} & \cdots & \dfrac{1}{a_{n,n-1}} & \dfrac{-a_{nn}}{a_{n,n-1}} \\ 0 & 0 & \cdots & 0 & 1 \end{bmatrix}.$$

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Manuscript received October 7, 1964.

[1] M. M. Milić, "Flow-graph evaluation of the characteristic polynomial of a matrix," *IEEE Trans. on Circuit Theory (Correspondence)*, vol. CT-11, pp. 423–424, September 1964.

[2] V. N. Faddeeva, *Computational Methods of Linear Algebra*. New York: Dover, 1959, pp. 166–176.